Cache memory

Memory address from processor

Main memory accessed if address not in cache

Cache

Compare with all stored addresses simultaneously

Address

Data

Main memory

Address found

Address not found in cache

Address location

[The Cache Memory](#)

SJ Ball

The Cache Memory:

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Benveniste,Peter A. Franaszek,John T. Robinson,2000 Abstract We consider a number of cache memory hierarchy design issues in systems with compressed random access memories C RAMs in which compression and decompression occur automatically to and from main memory Using a C RAM as main memory segments of main memory are stored in a compressed format and dynamically decompressed to handle cache misses at the next higher level of memory Design of main memory directory structures and storage allocation methods in such systems are described elsewhere here we focus on issues related to cache memory interfaces In particular if the cache line size of the cache or caches to which main memory data is transferred is different than the size of the unit of compression in main memory bandwidth and latency problems can occur Another issue is that of guaranteed forward progress that is ensuring that modified lines can be written to the compressed main memory so that the system can continue operation even if overall compression deteriorates We study several approaches for solving these problems using trace driven analysis to evaluate alternatives **Parallel and Distributed Simulation Systems** Richard M. Fujimoto,2000-01-03 From the preface page xv My goal in writing Parallel and Distributed Simulation Systems is to give an in depth treatment of technical issues concerning the execution of discrete event simulation programs on computing platforms composed of many processores interconnected through a network **SPARC RISC User's Guide** Ross Technology,1990 *Implementing Persistent Object Bases* Alan Dearle,Gail M. Shaw,Stanley Benjamin Zdonik,1991 Computer Design ,1987 *Microprocessor System Design Techniques* Richard Barnett,1991 **Computer Architecture and VAX Assembly Language Programming** James E. Brink,Richard J. Spillman,1987 Detailed coverage of architecture hardware topics such as CPU microprocessors large computer architecture and fault tolerance architecture makes this a valuable reference For computer science and electrical engineering professionals as well as VAX assembly language programmers **Organization and Analysis of Interleaved Memory Systems** Ki-Fung Calvin Cheung,1987 Operating Systems William Stallings,1998 Blending up to date theory with modern applications this book offers a comprehensive treatment of operating systems with an emphasis on internals and design issues The title provides a solid understanding of the key mechanisms of operating systems and types of design tradeoffs and decisions *The New A+ Certification Training Guide* Charles J. Brooks,1998 Electronic Design ,1983 **Peter Norton's Inside the PC** Peter Norton,John Goodman,1997 With advice from the experts a user friendly hands on approach and a 16 page full colour insert this book helps users better understand their PC realise its potential foresee possible problems and make the right decisions **A+ Certification Theory and Study Guide** Charles J. Brooks,1998 The A Certification is a testing program that certifies the competency of service technicians in the computer industry Earning A Certification means that you possess the knowledge skills and customer relations skills essential to be a successful computer service technician Candidates for this certification can use this guide to study from hundreds of test questions and take simulated tests on the CD ROM Proceedings Tencon ,1987 **Proceedings of the Trends in Electronics Conference** ,1987

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The Cache Memory Introduction

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