

VHDL MINI-REFERENCE

Reduced-verbosity version of [http://www.vhdl.org/vhdl-spec/vhdl.html](#)

PRIMARY DESIGN UNIT MODEL STRUCTURE

Each VHDL design unit comprises an **ENTITY** declaration and one or more **ARCHITECTURE**s. Each architecture defines a different implementation of model of a given design unit. The entity declaration defines the inputs to, and outputs from the model, and any **ports** or parameters used by the different implementations of the model.

Entity Declaration Format

```
ENTITY entity_name IS  
    port (port_declaration_list) ;  
    generic (generic_declaration_list) ;  
END ENTITY;
```

Each declaration format: **entity_name**, **port_declaration_list**, **generic_declaration_list**

- **entity_name** is used for model that updated with the model, carrying information into the model. (It is **not** required appear on the left hand side of a signal assignment.)
- **port_declaration_list** is used for model that read within the model, carrying information out of the model. (It is **not** required appear on the right hand side of a signal assignment.)
- **generic_declaration_list** carries information out of a model, but can be both updated and read within the model.
- **port** is conventional used can be both read and updated, with multiple update sources possible.

ports (A **port** is a VHDL visibility on design unit, but can only be defined from within the model, while **signals** is only defined from within both within and external to the model.

Examples

```
ENTITY example IS  
    port (a : in std_logic; b : in std_logic; c : out std_logic);  
    generic (g : integer := 10);  
END ENTITY;
```

Remember allow extra information to be communicated to external from the environment for all architectures of a design unit. These include being information (input, output, using block, port alias, and other parameters.

```
ENTITY example IS  
    port (a : in std_logic; b : in std_logic; c : out std_logic);  
    generic (g : integer := 10);  
END ENTITY;
```

VHDL Standard Packages

To make TEXTIO visible: use the package clause.

IEEE Standard 1164 Package

The package contained in the IEEE library supports multi-valued logic signals with four declarations and functions. To make it visible:

```
LIBRARY ieee;  
USE ieee.std_logic_1164;
```

VHDL IDENTIFIERS, NUMBERS, STRINGS, AND EXPRESSIONS

Identifiers

Identifiers in VHDL must begin with a letter, and may comprise any combination of letters, digits, and underscores. Note that VHDL internally converts all characters to lower case.

Examples

```
identifier: a_b_c_d_e_f_g_h_i_j_k_l_m_n_o_p_q_r_s_t_u_v_w_x_y_z_0_1_2_3_4_5_6_7_8_9_.
```

Numeric Constants

Numeric constants can be defined, and can be of any base (default is decimal). Numbers may include embedded underscores to improve readability.

Format: **integer_literal** (Base must be a decimal number)

Examples

```
integer_literal: 123456789;  
real_literal: 123.456789;  
string_literal: "A string literal, regardless of its content."
```

Bit String Literals

Bit string constants are are specified as fixed strings.

Examples

```
bit_string_literal: "01101001010101010101010101010101";  
bit_string_literal: "01101001010101010101010101010101";  
bit_string_literal: "01101001010101010101010101010101";
```

Example

```
entity_name: entity_name IS  
    port (port_declaration_list) ;  
    generic (generic_declaration_list) ;  
    architecture architecture_name of entity_name is  
        -- architecture body  
    end architecture_name;  
end entity_name;
```

Architecture

An **architecture** defines one particular implementation of a design unit, at some defined level of abstraction.

```
architecture_name of entity_name is  
    port_declaration_list  
    generic_declaration_list  
end;
```

Declaration include data types, constants, signals, bus, components, attributes, subprograms, and other information to be used by the implementation description. Comments also may describe a design unit at one or more levels of modeling abstraction, including **block**, **structure**, and/or **behavior**.

- **Behavioral Model** is structure of technology specific (usually written in sequential, procedural code).
- **Structural Model** is technology neutral, plus all control signals.
- **Structural Model** is hierarchical of components.

VHDL PACKAGES

A **VHDL package** contains subprograms, constant definitions, and/or type definitions to be used throughout one or more design units. Each package comprises a declaration section in which the constants (ie, **enumerated**), subprograms, constants, and types are declared, and a **package body** in which the subprogram implementations are defined, along with any internally used constants and types. The declaration section represents the portion of the package that is visible to the user of that package. The actual implementations of subprograms in the package are typically not referenced by the users of those subprograms.

Package Declaration Format

```
PACKAGE package_name IS  
    -- constant, subprogram, enumeration, type  
    -- package body (optional)  
END PACKAGE;
```

Examples

Arithmetic and Logical Expressions

Expressions in VHDL are similar to those of most high-level languages. Data elements must be of the type, or subtype of the same base type. Operators include the following:

- **Logical**: **and**, **or**, **nand**, **nor**, **xor**, **xnor**, **not**, **notwendig**, **notwendig**
- **Arithmetic**: **+**, **-**, *****, **/**, **mod**, **rem**, **div**, **trunc**, **round**, **ceil**, **floor**, **abs**
- **Concatenation**: **||**

Examples

```
a := 10 + 20;  
b := a - 5;  
c := a * 3;  
d := a / 2;
```

VHDL DATA TYPES

Each VHDL object must be classified as being of a specific data type. VHDL includes a number of predefined data types, and allows users to define custom data types as needed.

Predefined Scalar Data Types (single objects)

VHDL Standard

- **boolean**: **TRUE**, **FALSE**
- **character**: **'A'** through **'Z'**, **'a'** through **'z'**, **'0'** through **'9'**, **space**
- **integer**: **0** to **2147483647** (**INTEGER_MAX**) and **-2147483648** to **-1** (**INTEGER_MIN**)
- **real**: **0.0** to **3.4028235e+38** (**REAL_MAX**) and **-3.4028235e+38** to **-1e-39** (**REAL_MIN**)
- **time**: **0** to **4294967295** (**TIME_MAX**) and **-4294967295** to **-1** (**TIME_MIN**)

IEEE Standard 1164 package (ieee.std_logic_1164)

- **std_logic**: **'0'**, **'1'**, **'Z'**, **'0'**, **'1'**, **'Z'**, **'X'**, **'0'**, **'1'**, **'Z'**, **'X'**
- **std_logic_vector**: **(0 to 255)** **std_logic_vector**
- **std_logic_1164**: **'0'**, **'1'**, **'Z'**, **'0'**, **'1'**, **'Z'**, **'X'**, **'0'**, **'1'**, **'Z'**, **'X'**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**

Predefined VHDL Aggregate Data Types

- **std_logic_vector**: **(0 to 255)** **std_logic_vector**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**
- **std_logic_1164**: **(0 to 255)** **std_logic_1164**

IEEE Standard 1164 Aggregate Data Types

```
package_clause: package_name IS  
    port (port_declaration_list) ;  
    generic (generic_declaration_list) ;  
    architecture architecture_name of package_name is  
        -- architecture body  
    end architecture_name;  
end package_name;
```

Package Body Format

```
package_name: package_name IS  
    port (port_declaration_list) ;  
    generic (generic_declaration_list) ;  
    architecture architecture_name of package_name is  
        -- architecture body  
    end architecture_name;  
end package_name;
```

Examples

```
package_name: package_name IS  
    port (port_declaration_list) ;  
    generic (generic_declaration_list) ;  
    architecture architecture_name of package_name is  
        -- architecture body  
    end architecture_name;  
end package_name;
```

Package Visibility

To make all items of a package "visible" to a design unit, provide the desired design unit with a **use** statement.

Example

```
LIBRARY ieee;  
USE ieee.std_logic_1164;
```

A **use** statement may precede the declaration of any entity or architecture which is to refer items from the package. The **use** statement precedes the entity declaration, the package is also visible to the architecture.

User-Developed Packages

Create user-developed packages in your current working library. To make it visible:

```
LIBRARY user_package;  
USE user_package;
```

Note: **use** and **use work** (your current working library) can be used without **library**. The **LIBRARY** statement is needed to make the **use** (library) visible and available.

Example

Example (ieee.std_logic_1164)

- **std_logic**: **'0'**, **'1'**, **'Z'**, **'0'**, **'1'**, **'Z'**, **'X'**, **'0'**, **'1'**, **'Z'**, **'X'**
- **std_logic_vector**: **(0 to 255)** **std_logic_vector**

Examples

```
LIBRARY ieee;  
USE ieee.std_logic_1164;  
LIBRARY user_package;  
USE user_package;
```

User-Defined Enumeration Types

An enumerated data type can be created by explicitly listing all possible values.

Example

```
enum_type: type enum_type IS  
    value1, value2, value3, value4;  
end enum_type;
```

Other user-defined types

Custom data types can include arrays, enumerated and unconstrained, and record structures.

- **enumerated** array: **value1** and **value2** values are specified.
- **unconstrained** array: **value1** and **value2** values are specified when a signal or variable of that type is declared.
- **subtype**: A selected subset of values of a given type. Elements of different subtypes having the same base type may be combined to expressions (elements of different types cannot). Subtypes can be created to select out of larger values having structure.

Aliases

An **alias** defines an alternate name for a signal or part of a signal. Aliases are often useful to refer to selected slices of a signal.

Example

```
signal_declaration: signal_declaration IS  
    port (port_declaration_list) ;  
    architecture architecture_name of signal_declaration is  
        -- architecture body  
    end architecture_name;
```

VHDL OBJECTS: CONSTANTS, VARIABLES, AND SIGNALS

Vhdl Designers Reference

Peter J. Ashenden



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