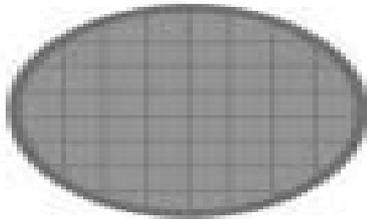
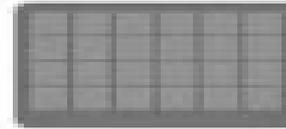


## WHAT IS A WAFER?



### SILICON WAFER

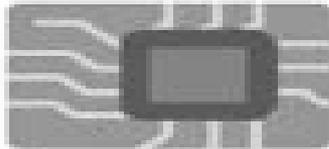
A thin, round slice  
of silicon crystal



### CHIP

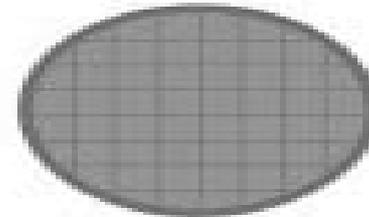
A small piece cut  
from a wafer

## WHY WAFER-SCALE INTEGRATION?



### FAST COMMUNICATION

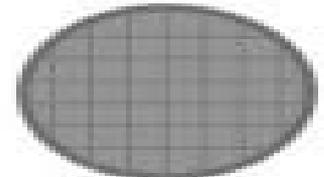
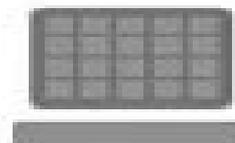
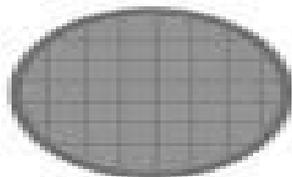
All components are  
directly connected



### MORE COMPUTING POWER

The whole wafer acts  
as a single chip

## THE PROCESS



SILICON WAFER

PHOTOLITHOGRAPHY

ETCHING

WSI CHIP

# Wafer Scale Integration

**Xiaolong Qi**



## **Wafer Scale Integration:**

**Wafer Scale Integration** Earl E. Swartzlander Jr., 2012-12-06 Wafer Scale Integration WSI is the culmination of the quest for larger integrated circuits In VLSI chips are developed by fabricating a wafer with hundreds of identical circuits testing the circuits dicing the wafer and packaging the good dice In contrast in WSI a wafer is fabricated with several types of circuits generally referred to as cells with multiple instances of each cell type the cells are tested and good cells are interconnected to realize a system on the wafer Since most signal lines stay on the wafer stray capacitance is low so that high speeds are achieved with low power consumption For the same technology a WSI implementation may be a factor of five faster dissipate a factor of ten less power and require one hundredth to one thousandth the volume Successful development of WSI involves many overlapping disciplines ranging from architecture to test design to fabrication including laser linking and cutting multiple levels of interconnection and packaging This book concentrates on the areas that are unique to WSI and that are as a result not well covered by any of the many books on VLSI design A unique aspect of WSI is that the finished circuits are so large that there will be defects in some portions of the circuit Accordingly much attention must be devoted to designing architectures that facilitate fault detection and reconfiguration to of WSI include fabrication circumvent the faults Other unique aspects technology and packaging

Wafer-Level Integrated Systems Stuart K. Tewksbury, 2012-12-06 From the perspective of complex systems conventional Ie s can be regarded as discrete devices interconnected according to system design objectives imposed at the circuit board level and higher levels in the system implementation hierarchy However silicon monolithic circuits have progressed to such complex functions that a transition from a philosophy of integrated circuits Ie s to one of integrated systems is necessary Wafer scale integration has played an important role over the past few years in highlighting the system level issues which will most significantly impact the implementation of complex monolithic systems and system components Rather than being a revolutionary approach wafer scale integration will evolve naturally from VLSI as defect avoidance fault tolerance and testing are introduced into VLSI circuits Successful introduction of defect avoidance for example relaxes limits imposed by yield and cost on Ie dimensions allowing the monolithic circuit s area to be chosen according to the natural partitioning of a system into individual functions rather than imposing area limits due to defect densities The term wafer level is perhaps more appropriate than wafer scale A wafer level monolithic system component may have dimensions ranging from conventional yield limited Ie dimensions to full wafer dimensions In this sense wafer scale merely represents the obvious upper practical limit imposed by wafer sizes on the area of monolithic circuits The transition to monolithic wafer level integrated systems will require a mapping of the full range of system design issues onto the design of monolithic circuit

**Frontiers of Computing Systems Research** Stuart K. Tewksbury, 2012-12-06 Computing systems researchers confront two serious problems 1 The increasingly monolithic or pseudo monolithic integration of complex computing functions and systems imposes an environment which integrates advanced principles and

techniques from a broad variety of fields Researchers not only must confront the increased complexity of topics in their specialty field but also must develop a deeper general understanding of a broadening number of fields 2 There has been a proliferation of journals books workshops and conferences through which research results are reported Remaining familiar with recent advances in our specific fields is a major challenge Casually browsing through journals and conference proceedings to remain aware of developments in areas outside our specialization has become an even greater challenge Frontiers of Computing Systems Research has been established to address these two issues With the assistance of an advisory board of experts from a wide variety of specialized areas we hope to provide roughly annual volumes of invited chapters on a broad range of topics and designed for an interdisciplinary research audience No single volume can cover all the relevant topics and no single article can convey the full set of directions being pursued within a given topic For this reason a chapter listing technical reports available from universities is also included Often such unpublished reports are designed for a general research audience and provide a good informal look at trends in specialized research topics

**Wafer-scale Integration of Systolic Arrays** Frank Thomson Leighton, Charles E. Leiserson, 1983 VLSI technologies are fast developing wafer scale integration Rather than partitioning a silicon wafer into chips as is usually done the idea behind wafer scale integration is to assemble an entire system or network of chips on a single wafer thus avoiding the costs and performance loss associated with individual packaging of chips A major problem with assembling a large system of microprocessors on a single wafer however is that some of the processors or cells on the wafer are likely to be defective In the paper we describe practical procedures for integrating wafer scale systems around such faults The procedures are designed to minimize the length of the longest wire in the system thus minimizing the communication time between cells Although the underlying network problems are NP complete we prove that the procedures are reliable by assuming a probabilistic model of cell failure We also discuss applications of this work to problems in VLSI layout theory graph theory fault tolerant systems and planar geometry

**Electronic Materials Handbook**, 1989-11-01 Volume 1 Packaging is an authoritative reference source of practical information for the design or process engineer who must make informed day to day decisions about the materials and processes of microelectronic packaging Its 117 articles offer the collective knowledge wisdom and judgement of 407 microelectronics packaging experts authors co authors and reviewers representing 192 companies universities laboratories and other organizations This is the inaugural volume of ASMAs all new Electronic Materials Handbook series designed to be the Metals Handbook of electronics technology In over 65 years of publishing the Metals Handbook ASM has developed a unique editorial method of compiling large technical reference books ASMAs access to leading materials technology experts enables to organize these books on an industry consensus basis Behind every article is an author who is a top expert in its specific subject area This multi author approach ensures the best most timely information throughout Individually selected panels of 5 and 6 peers review each article for technical accuracy

generic point of view and completeness Volumes in the Electronic Materials Handbook series are multidisciplinary to reflect industry practice applied in integrating multiple technology disciplines necessary to any program in advanced electronics Volume 1 Packaging focusing on the middle level of the electronics technology size spectrum offers the greatest practical value to the largest and broadest group of users Future volumes in the series will address topics on larger integrated electronic assemblies and smaller semiconductor materials and devices size levels

**Wafer Scale Integration, III**  
Mariagiovanna Sami, Fausto Distante, 1990 The purpose of this book is to give an up to date presentation of architectures and technologies for wafer scale integration As such it is an overview of the work of the leading research centers active in this area and an outline of expected evolution and progress in the subject New technological solutions are envisioned while the use of optical technologies for interconnections promises to overcome one of the main restrictions to architectures on a wafer the extension of quick prototyping solutions to the wafer dimension allows the introduction of wafer scale systems in educational environments as well as in applications where a quick result and limited production would make traditional silicon solutions unacceptable Regarding architectures and their applications three different lines of approach can be identified Evolutive solutions are proposed mainly concerning array architectures and restructuring techniques Innovative architectures are presented several papers dealing with neural nets There are also architectures designed not just for experimental reasons but for industrial production Overall non numerical applications predominate

Defect and Fault Tolerance in VLSI Systems Israel Koren, 2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized

**Defect and Fault Tolerance in VLSI Systems** C.H. Stapper, V.K. Jain, Gabriele Saucier, 2013-06-29 Higher circuit densities increasingly more complex application objectives and advanced packaging

technologies have substantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems. The goals of defect tolerance and fault tolerance are yield enhancement and improved reliability. The emphasis on this area has resulted in a new field of interdisciplinary scientific research. In fact, advanced methods of defect fault control and tolerance are resulting in enhanced manufacturability and productivity of integrated circuit chips. VLSI systems and wafer scale integrated circuits. In 1987, Dr. W. Moore organized an International Workshop on Designing for Yield at Oxford University. Edited papers of that workshop were published in reference II. The participants in that workshop agreed that meetings of this type should be continued preferably on a yearly basis. It was Dr. I. Koren who organized the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield, Massachusetts the next year. Selected papers from that workshop were published as the first volume of this series. 21 *Beam Processing Technologies* Norman G. Einspruch, S. S. Cohen, Raj N. Singh, 2014-12-01. *Beam Processing Technologies* is a collection of papers that deals with the miniaturization of devices that will be faster, consume less power, and cost less per operation or fabrication. One paper discusses metal oxide semiconductor (MOS) integrated circuit technology including the operation of devices whose lateral and vertical dimensions are scaled down. If the devices' silicon doping profiles are increased by the same scale factor, they can operate on lower voltages and currents with the same performance. Another paper describes laser beam processing and wafer scale integration as techniques to increase the number of devices on a silicon chip. Electron beam technologies can be used in many fabrication processes such as in microlithography, selective oxidation, doping, metrology, ion beam applications, etc. depend on the presence of the ion introduced into the device, e.g., implantation, doping, on pseudoelastic collisions, e.g., physical sputtering or crystal damage, and on inelastic scattering, e.g., polymer resist exposure. Silicon molecular beam epitaxy (SiMBE) can also grow high quality layers at low temperature, particularly concerning germanium, especially as regards the growth system design and utilization of n and p type doping. Chemical beam epitaxy (CBE) is another epitaxial growth technique that can surpass MBE and metal organic chemical vapor deposition (MOCVD). The collection is suitable for chemical engineers, industrial physicists, and researchers whose work involves micro fabrication and development of integrated circuits. Wafer Scale Integration of Parallel Processors Kye Sherrick Hedlund, PURDUE UNIV LAFAYETTE IN DEPT OF COMPUTER SCIENCES., 1982. This research examines the problem of construction chips up to the size of the wafer wafer scale integration that operate correctly despite the occurrence of such flaws. We concentrate on a particular family of parallel processors, configurable highly parallel CHiP processors. The key problem in the implementation of wafer scale integration is structuring the wafer so that only the functional PEs are connected together. A methodology, the two level hierarchy, that efficiently and economically solves the structuring problem for CHiP processors is presented. The principle elements are the use of column exclusion with high yield building blocks that contain redundant components. This approach limits the performance degradation due to structuring and allows the structuring problem to be solved with tractable computational

effort Since the yield of building blocks must be high for the two level hierarchy to be a practical approach yield phenomena are investigated in detail Wafer scale integration ; 1 ,1986 Wafer scale integration ; 2 ,1987 Wafer scale integration ; 3 ,1989 Wafer Scale Integration Glenn Chapman,R. Mike Lea,Stuart Tewksbury,1994 *Metallurgical Coatings 1988* R Krutenat,2012-12-02 Metallurgical coatings 1988 is a compilation of the proceedings of the 15th International Conference on Metallurgical Coatings This volume is divided into four parts which deal with synthesis and properties of coatings used in microelectronic applications methods of characterizing coatings and modified surfaces protective coatings for magnetic and optical thin film media and thick and thin film sensors The first part of this volume is further subdivided into five sections focusing on thin film barrier layers metallization for VLSI circuits thin films used in packaging technology new materials and emerging technologies and synthesis and microstructure of high Tc superconductors The second part is also subdivided into four sections each presenting different methods such as the surface and thin film analysis techniques microstructural characterization techniques mechanical properties of films and coatings and non destructive characterization techniques Part three discusses the preparation and characterization of reactively sputtered silicon nitride thin films the bond structures and properties of chemically vapor deposited amorphous SiC and the wear of Co Ni thin film magnetic recording tape against metallic and ceramic surfaces Finally this volume explores the insert mounted thin film sensors for real time **"Wafer Scale Integration, International Conference On".** , 1991 Proceedings Michael J. Little,Vijay K. Jain,1991 **Manufacturing Yield Evaluation of VLSI/WSI Systems** Bruno Ciciani,1995 A practical understanding of these concepts and their application can help to reduce the chance of having device failures *Wafer Scale Integration, II* R. M. Lea,1988 *Wafer Scale Integration* Joe E. Brewer,1993

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