



ADDRESS REGISTER
1,000 bits

WORD-IN REGISTER
1,000 bits

x 1 0 0 ... 1 0 1

w 0 1 0 ... 1 1 0

1,000,000 hard locations

	0	1	0		1	0	1
	1	0	1		0	0	1
	0	1	0		0	1	1
	0	0	0		1	0	1
	1	1	1		0	0	1
	0	0	0		1	1	0
	A						
	ADDRESS MATRIX						
	M hard addresses						
	1	1	1		0	0	0
	1	0	0		1	0	0
	1	0	0		0	1	0
M	0	1	1		0	1	1

d

501
444
550
447
493
531
·
·
·
480
446
512
498

y

0
1
0
1
0
0
·
·
·
0
1
0
0
0

M

U

0	2	-2		4	0	0
-1	-1	-1		1	3	-1
1	1	-3		-1	1	1
-2	4	2		0	2	0
-1	1	1		-3	-1	-1
2	0	-4		0	2	0
C						
CONTENTS MATRIX						
$M \times U$ counters						
1	3	-1		3	-3	5
-1	1	-1		1	1	-1
2	0	-4		0	6	-4
0	0	0		0	0	0

z

-445	379	-201	·	·	·	77	611	-517
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z 0 1 0 ... 1 1 0

WORD-OUT REGISTER
1,000 bits

Sparse Distributed Memory

Shambulingappa V. Chinvar



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