1–10 metal layers

≥2 layers of active devices

Device layer 2

Vertical interconnect

Single device layer

Device layer 1

Silicon

Three Dimensional Integrated Circuit Layout

J Elliott

Three Dimensional Integrated Circuit Layout:

 Three-dimensional Integrated Circuit Design Vasilis F. Pavlidis,Eby G. Friedman,2010-07-28 With vastly increased complexity and functionality in the nanometer era i e hundreds of millions of transistors on one chip increasing the performance of integrated circuits has become a challenging task Connecting effectively interconnect design all of these chip elements has become the greatest determining factor in overall performance 3 D integrated circuit design may offer the best solutions in the near future This is the first book on 3 D integrated circuit design covering all of the technological and design aspects of this emerging design paradigm while proposing effective solutions to specific challenging problems concerning the design of 3 D integrated circuits A handy comprehensive reference or a practical design guide this book provides a sound foundation for the design of 3 D integrated circuits Demonstrates how to overcome interconnect bottleneck with 3 D integrated circuit design leading edge design techniques offer solutions to problems performance power consumption price faced by all circuit designers The FIRST book on 3 D integrated circuit design provides up to date information that is otherwise difficult to find Focuses on design issues key to the product development cycle good design plays a major role in exploiting the implementation flexibilities offered in the 3 D Provides broad coverage of 3 D integrated circuit design including interconnect prediction models thermal management techniques and timing optimization offers practical view of designing 3 D circuits   Three-Dimensional Integrated Circuit Layout Andrew Harter,1991-11-28 First published in 1991 this thesis concentrates upon the design of three dimensional rather than the traditional two dimensional circuits The theory behind such circuits is presented in detail together with experimental results   **Three-Dimensional Integrated Circuit Design** Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2009-12-02 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs   **Three-Dimensional Integrated**

Circuit Design Vasilis F. Pavlidis,Ioannis Savidis,Eby G. Friedman,2017-07-04 Three Dimensional Integrated Circuit Design Second Eition expands the original with more than twice as much new content adding the latest developments in circuit models temperature considerations power management memory issues and heterogeneous integration 3 D IC experts Pavlidis Savidis and Friedman cover the full product development cycle throughout the book emphasizing not only physical design but also algorithms and system level considerations to increase speed while conserving energy A handy comprehensive reference or a practical design guide this book provides effective solutions to specific challenging problems concerning the design of three dimensional integrated circuits Expanded with new chapters and updates throughout based on the latest research in 3 D integration Manufacturing techniques for 3 D ICs with TSVs Electrical modeling and closed form expressions of through silicon vias Substrate noise coupling in heterogeneous 3 D ICs Design of 3 D ICs with inductive links Synchronization in 3 D ICs Variation effects on 3 D ICs Correlation of WID variations for intra tier buffers and wires Offers practical guidance on designing 3 D heterogeneous systems Provides power delivery of 3 D ICs Demonstrates the use of 3 D ICs within heterogeneous systems that include a variety of materials devices processors GPU CPU integration and more Provides experimental case studies in power delivery synchronization and thermal characterization **Three-Dimensional Integrated Circuit Design** Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2009-12-10 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs **Three-Dimensional Integrated Circuit Design** Yuan Xie,Jingsheng Jason Cong,Sachin Sapatnekar,2010-05-19 We live in a time of great change In the electronics world the last several decades have seen unprecedented growth and advancement described by Moore s law This observation stated that transistor density in integrated circuits doubles every 1 5 2 years This came with the simultaneous improvement of individual device perf mance as well as the reduction of device

power such that the total power of the resulting ICs remained under control No trend remains constant forever and this is unfortunately the case with Moore s law The trouble began a number of years ago when CMOS devices were no longer able to proceed along the classical scaling trends Key device parameters such as gate oxide thickness were simply no longer able to scale As a result device o state currents began to creep up at an alarming rate These continuing problems with classical scaling have led to a leveling off of IC clock speeds to the range of several GHz Of course chips can be clocked higher but the thermal issues become unmanageable This has led to the recent trend toward microprocessors with mul ple cores each running at a few GHz at the most The goal is to continue improving performance via parallelism by adding more and more cores instead of increasing speed The challenge here is to ensure that general purpose codes can be ef ciently parallelized There is another potential solution to the problem of how to improve CMOS technology performance three dimensional integrated circuits 3D ICs **Three-Dimensional Integrated Circuits** Guangyu Sun,Yibo Chen,Xiangyu Dong,Yuan Xie,Jin Ouyang,2011-05 Presents the background on 3D integration technology and shows the major benefits offered by 3D integration EDA design tools and methodologies for 3D ICs are reviewed The cost of 3D integration is also analyzed **Three Dimensional System Integration** Antonis Papanikolaou,Dimitrios Soudris,Riko Radojcic,2010-12-07 Three dimensional 3D integrated circuit IC stacking is the next big step in electronic system integration It enables packing more functionality as well as integration of heterogeneous materials devices and signals in the same space volume This results in consumer electronics e g mobile handheld devices which can run more powerful applications such as full length movies and 3D games with longer battery life This technology is so promising that it is expected to be a mainstream technology a few years from now less than 10 15 years from its original conception To achieve this type of end product changes in the entire manufacturing and design process of electronic systems are taking place This book provides readers with an accessible tutorial on a broad range of topics essential to the non expert in 3D System Integration It is an invaluable resource for anybody in need of an overview of the 3D manufacturing and design chain Design for High Performance, Low Power, and Reliable 3D Integrated Circuits Sung Kyu Lim,2012-11-27 This book provides readers with a variety of algorithms and software tools dedicated to the physical design of through silicon via TSV based three dimensional integrated circuits It describes numerous manufacturing ready GDSII level layouts of TSV based 3D ICs developed with the tools covered in the book This book will also feature sign off level analysis of timing power signal integrity and thermal analysis for 3D IC designs Full details of the related algorithms will be provided so that the readers will be able not only to grasp the core mechanics of the physical design tools but also to be able to reproduce and improve upon the results themselves This book will also offer various design for manufacturability DFM design for reliability DFR and design for testability DFT techniques that are considered critical to the physical design process *Design Methodology for Three-dimensional CMOS Integrated Circuits* Branislav Jovan Vajdic,1984 3D IC Stacking Technology Banqiu Wu,Ajay Kumar,Sesh Ramaswami,2011-07-07 The latest

advances in three dimensional integrated circuit stacking technology With a focus on industrial applications 3D IC Stacking Technology offers comprehensive coverage of design test and fabrication processing methods for three dimensional device integration Each chapter in this authoritative guide is written by industry experts and details a separate fabrication step Future industry applications and cutting edge design potential are also discussed This is an essential resource for semiconductor engineers and portable device designers 3D IC Stacking Technology covers High density through silicon stacking TSS technology Practical design ecosystem for heterogeneous 3D IC products Design automation and TCAD tool solutions for through silicon via TSV based 3D IC stack Process integration for TSV manufacturing High aspect ratio silicon etch for TSV Dielectric deposition for TSV Barrier and seed deposition Copper electrodeposition for TSV Chemical mechanical polishing for TSV applications Temporary and permanent bonding Assembly and test aspects of TSV technology

   Design of 3D Integrated Circuits and Systems Rohit Sharma,2018-09-03 Three dimensional 3D integration of microsystems and subsystems has become essential to the future of semiconductor technology development 3D integration requires a greater understanding of several interconnected systems stacked over each other While this vertical growth profoundly increases the system functionality it also exponentially increases the design complexity Design of 3D Integrated Circuits and Systems tackles all aspects of 3D integration including 3D circuit and system design new processes and simulation techniques alternative communication schemes for 3D circuits and systems application of novel materials for 3D systems and the thermal challenges to restrict power dissipation and improve performance of 3D systems Containing contributions from experts in industry as well as academia this authoritative text Illustrates different 3D integration approaches such as die to die die to wafer and wafer to wafer Discusses the use of interposer technology and the role of Through Silicon Vias TSVs Presents the latest improvements in three major fields of thermal management for multiprocessor systems on chip MPSoCs Explores ThruChip Interface TCI NAND flash memory stacking and emerging applications Describes large scale integration testing and state of the art low power testing solutions Complete with experimental results of chip level 3D integration schemes tested at IBM and case studies on advanced complementary metal oxide semiconductor CMOS integration for 3D integrated circuits ICs Design of 3D Integrated Circuits and Systems is a practical reference that not only covers a wealth of design issues encountered in 3D integration but also demonstrates their impact on the efficiency of 3D systems   *System Design of Multi-Layer (Three Dimensional) Integrated Circuits* J. F. Gibbons,STANFORD UNIV CA STANFORD ELECTRONICS LABS.,1985 Research carried out on beam processing of semiconductors led to the concept of a three dimensional integrated circuit It was shown that MOS devices could be made on both sides of a laser recrystallized thin film of silicon deposited on an insulating substrate SOI and also on vertically arranged recrystallized silicon films separated by insulating layers of silicon dioxide and or silicon nitride oxide combinations It follows from these observations that integrated circuits can be made by vertically interconnecting devices made on separate layers Such circuits could lead to

improved packing density which would be important for memory applications and possibly to increased circuit speed which would be important for logic application   **The Cumulative Book Index** ,1992 A world list of books in the English language   **Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications** ,1999   **Proceedings** Asim Smailagic,Nagarajan Ranganathan,2003 The Symposium covers a range of topics from VLSI circuits systems and design methods to system level design and system on chip issues to bringing VLSI experience to new areas and technologies like nano and molecular devices Future design methodologies are also one of the key topics at the symposium as well as new CAD tools to support them Over almost two decades this has been an unique forum promoting multidisciplinary research and new visionary research approaches in the area of VLSI   **Proceedings** ,2005   *Thermal-driven Placement in 3-dimensional Integrated Circuits* Wei Li,2007   **Three Dimensional Integrated Circuit Design and Test** Jing Xie,2015 The emerging three dimensional integrated circuits 3D ICs is one of the most promising solutions for future IC designs 3D stacking enables much higher memory bandwidth and much lower overhead in multi power domain design which provides solutions for chip multiprocessor design in mitigating the memory wall and dark silicon problem At the same time 3D technology leads to new opportunities and challenges in the field of circuit and system design techniques EDA tools and chip testing mechanism This dissertation presents two killer applications for the modern 3D system and one 3D testing solution The first contribution of this dissertation is to propose a killer application for TSV based system the 3D memory stacking This dissertation presents a 3D memory stacking system that leverages the massive number of TSVs between memory layers to help high bandwidth checkpointing restore To validate the proposed scheme 2 layer TSV based SRAM SRAM 3D stacked chip is implemented to mimic the high bandwidth and fast data transfer from one memory layer to another memory layer so that the in memory checkpointing restore scheme can be enabled for the future exascale computing The capacity of each SRAM layer is 1 Mbit Each layer contains 64 banks with each bank contains 256 words and the word length is 64 bit The final footprint including I O pad is 2 9mm X 2mm The SRAM dies were taped out in GlobalFoundries using its 130nm low power process and the 3D stacking was done by using Tezzaron s TSV technology The prototyping chip can perform checkpointing restore at the speed of 4K cycle with 1Ghz clock This dissertation also gives an applicable solution for 3D testing Testing for 3D ICs based on through silicon via TSV is one of the major challenges for improving the system yield and reducing the overall cost The lack of pads on most tiers and the mechanical vulnerability of tiers after wafer thinning make it difficult to perform 3D Known Good Die KGD test with the existing 2D IC probing methods This dissertation presents a novel and time efficient 3D testing flow In this Known Good Stack KGS flow a yield aware TSV defect searching and replacing strategy is introduced The Build in Self Test BIST design with TSV redundancy scheme help improve the system yield for today s imperfect TSV fabrication process Our study shows that less than 6 redundant TSVs is enough to increase the TSV yield to 98% for a TSV cluster with a size under 16 X 16 with relatively low initial TSV yield The average TSV cluster

testing and self fixing time is about 3 16 testing cycle depending on the initial TSV yield The second killer application for 3D system in this dissertation is multi power domain system design utilizing the monolithic technology Optimizing energy consumption for electronic systems has been an important design consideration Among all the techniques multi power domain design is a widely used one for low power and high performance applications In order to perform the data transfer between these different power domains we needs a cross power domain interface CPDI The existing level conversion flip flop LCFF structures all require dual power rails which results in large area and performance overhead We proposed a scan able CPDI circuit utilizing monolithic 3D technology This interface functions as a flip flop and provides reliable data conversion from one power domain to another It also has built in scan feature which makes it testable Our design separates power rails in each tier substantially reduced physical design complexity and area penalty The design is implemented in a 20nm 28nm and 45nm low power technology It shows 20% 35% smaller D to Q comparing with normal designs The proposed design also shows scalability and better energy consumption than precious LCFF design Finally we presented a dual power domain deep pipeline circuit architecture for future power efficient systems We reduce the power consumption by putting all the combinational logics in a lower power domain while all the FFs and clock network operate at normal voltage for smaller insertion delay and better clock control In order to realize these functions and system benefits we proposed a novel level conversion flip flop omega design which has 30% insertion delay than the normal flop design and could be easily integrated into today s synthesis flow This work provides guideline on how to design a dual power domain system with less power under the same system throughput requirement A system level estimation shows that the 3D dual power supply system could consume about 15% less energy by using our design methodology   Berkeley Technology Law Journal ,2000

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