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Osman S. Unsal, Israel Koren, System-Level
Power-Aware Design Techniques in Real-
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No. 7, July 2003.

Systemlevel Design Techniques For Energyefficient Embedded Systems

Sanguthevar Rajasekaran, John Reif



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applications computer networks cyber trust and security wireless networks as well as mobile computing and bioinformatics

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Sanguthevar Rajasekaran,John Reif,2007-12-20 The ability of parallel computing to process large data sets and handle time consuming operations has resulted in unprecedented advances in biological and scientific computing modeling and simulations Exploring these recent developments the Handbook of Parallel Computing Models Algorithms and Applications provides comprehensive coverage on a **Ambient Intelligence** Werner Weber,Jan Rabaey,Emile H.L. Aarts,2005-12-12

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ISLPED'03, 2003 **IEEE Workshop on Signal Processing Systems**, 1997 **Sixth IEEE International High-Level Design Validation and Test Workshop**, 2001. Eighteen full papers and eight short presentations from international engineers and researchers discuss current developments, new methodologies, and emerging trends in design verification and test. The focus of the sixth conference was on hardware/software embedded systems and system-on-chips. Topics include, for example, the automatic validation of pipeline specifications, the use of sequential ATPG for model checking, formal verification of the Pentium 4 multiplier, and using cutwidth to improve symbolic simulation and Boolean satisfiability. The volume is not indexed. c Book News Inc. **18th International Conference on VLSI Design** International Conference on VLSI Design, 2005 **Design Techniques for Energy-efficient Embedded and Mobile Computing Systems** Keith S. Vallerio, 2004 **The British National Bibliography** Arthur James Wells, 2004

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