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Introduction to Logic Synthesis using Verilog HDL Robert B. Reese, Mitchell A. Thornton, 2006-12-01 Introduction to Logic Synthesis Using Verilog HDL explains how to write accurate Verilog descriptions of digital systems that can be synthesized into digital system netlists with desirable characteristics The book contains numerous Verilog examples that begin with simple combinational networks and progress to synchronous sequential logic systems Common pitfalls in the development of synthesizable Verilog HDL are also discussed along with methods for avoiding them The target audience is anyone with a basic understanding of digital logic principles who wishes to learn how to model digital systems in the Verilog HDL in a manner that also allows for automatic synthesis A wide range of readers from hobbyists and undergraduate students to seasoned professionals will find this a compelling and approachable work The book provides concise coverage of the material and includes many examples enabling readers to quickly generate high quality synthesizable Verilog models

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SystemVerilog For Design Stuart Sutherland, Simon Davidmann, Peter Flake, 2013-12-01 SystemVerilog is a rich set of extensions to the IEEE 1364 2001 Verilog Hardware Description Language Verilog HDL These extensions address two major aspects of HDL based design First modeling very large designs with concise accurate and intuitive code Second writing high level test programs to efficiently and effectively verify these large designs This book SystemVerilog for Design addresses the first aspect of the SystemVerilog extensions to Verilog Important modeling

features are presented such as two state data types enumerated types user defined types structures unions and interfaces Emphasis is placed on the proper usage of these enhancements for simulation and synthesis A companion to this book SystemVerilog for Verification covers the second aspect of SystemVerilog Verilog HDL Synthesis Jayaram Bhasker,1998

The Leading Quickstart Guide to Verilog on the Planet Nitin Srimal,2020-05-16 The book is intended to provide readers with a quick start guide to Verilog language Verilog has become the de facto standard in hardware description languages HDLs The book is designed as a learning workshop and includes numerous exercises examples and labs On completion the readers shall have a working knowledge of the Verilog language The readers shall be able to read and write verilog RTL level models The readers shall understand how to write synthesizable code The readers shall get familiar with creation and use of test benches **Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL** Michael D. Ciletti,1999 Verilog

aims to introduce new users to the language of Verilog with instruction on how to write hardware descriptions in Verilog in a style that can be synthesized by readily available synthesis tools Offers clear exposition of the Verilog hardware description language This book is written in a style that allows the user who has no previous background with hardware description languages HDLs to become skillful with the language Features treatment of synthesis friendly descriptive styles An excellent book for self study reference seminars and workshops on the subject **Verilog Quickstart** James M. Lee,1997 Explains to engineers and students how to use the Verilog hardware description language to simulate debug and document a design based on Lee s course at the University of California Sets out some of the formal syntax and definitions demonstrates use of the language with over 100 examples then looks at how style affects the choice of constructs for modeling a design Neither a comprehensive reference nor a theoretical account Assumes a background in hardware design The 3 5 disk contains the example files in both DOS and UNIX formats No bibliography Annotation copyrighted by Book News Inc Portland OR

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