Software Synthesis From Dataflow Graphs

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Software Synthesis From Dataflow Graphs:

Software Synthesis from Dataflow Graphs Shuvra S. Bhattacharyya,Praveen K. Murthy,Edward A. Lee,2012-12-06 Software Synthesis from Dataflow Graphs addresses the problem of generating efficient software implementations from applications specified as synchronous dataflow graphs for programmable digital signal processors DSPs used in embedded real time systems The advent of high speed graphics workstations has made feasible the use of graphical block diagram programming environments by designers of signal processing systems A particular subset of dataflow called Synchronous Dataflow SDF has proven efficient for representing a wide class of unirate and multirate signal processing algorithms and has been used as the basis for numerous DSP block diagram based programming environments such as the Signal Processing Workstation from Cadence Design Systems Inc COSSAP from Synopsys both commercial tools and the Ptolemy environment from the University of California at Berkeley A key property of the SDF model is that static schedules can be determined at compile time This removes the overhead of dynamic scheduling and is thus useful for real time DSP programs where throughput requirements are often severe Another constraint that programmable DSPs for embedded systems have is the limited amount of on chip memory Off chip memory is not only expensive but is also slower and increases the power consumption of the system hence it is imperative that programs fit in the on chip memory whenever possible Software Synthesis from Dataflow Graphs reviews the state of the art in constructing static memory optimal schedules for programs expressed as SDF graphs Code size reduction is obtained by the careful organization of loops in the target code Data buffering is optimized by constructing the loop hierarchy in provably optimal ways for many classes of SDF graphs The central result is a uniprocessor scheduling framework that provably synthesizes the most compact looping structures called singleappearance schedules for a certain class of SDF graphs In addition algorithms and heuristics are presented that generate single appearance schedules optimized for data buffering usage Numerous practical examples and extensive experimental data are provided to illustrate the efficacy of these techniques **Handbook of Signal Processing Systems** Shuvra S. Bhattacharyya,Ed F. Deprettere,Rainer Leupers,Jarmo Takala,2013-06-20 Handbook of Signal Processing Systems is organized in three parts The first part motivates representative applications that drive and apply state of the art methods for design and implementation of signal processing systems the second part discusses architectures for implementing these applications the third part focuses on compilers and simulation tools describes models of computation and their associated design tools and methodologies This handbook is an essential tool for professionals in many fields and researchers of all levels EDA for IC System Design, Verification, and Testing Louis Scheffer,Luciano Lavagno,Grant Martin,2018-10-03 Presenting a comprehensive overview of the design automation algorithms tools and methodologies used to design integrated circuits the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes The first volume EDA for IC System Design Verification and Testing thoroughly examines system level design microarchitectural design logical

verification and testing Chapters contributed by leading experts authoritatively discuss processor modeling and design tools using performance metrics to select microprocessor cores for IC designs design and verification languages digital simulation hardware acceleration and emulation and much more Save on the complete set *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology* ,1999 *Software and Compilers for Embedded Systems* Henk Schepers,2004-08-23 This book constitutes the refereed proceedings of the 8th International Workshop on Software and Compilers for Embedded Systems SCOPES 2004 held in Amsterdam The Netherlands in September 2004 The 17 revised full papers presented were carefully reviewed and selected from close to 50 submissions The papers are organized in topical sections on application synthesis data flow analysis data partitioning task scheduling and code generation Readings in Hardware/Software Co-Design Giovanni De Micheli,Rolf Ernst,Wayne Wolf,2002 This title serves as an introduction ans reference for the field with the papers that have shaped the hardware software co design since its inception in the early 90s

Proceedings, Fifth IEEE International Symposium on High Assurance Systems Engineering (HASE 2000) ,2000 The proceedings from this November 2000 conference in Albuquerque New Mexico feature 46 papers by computer scientists working with universities private companies and government agencies from around the world Topics include test based comprehension failure prediction models symposia benefits *IEEE Workshop on Signal Processing Systems* ,1998

IEEE International Conference on Application-Specific Systems, Architectures and Processors Lothar Thiele (Computer scientist),1997 These conference papers on computer hardware and design and testing include coverage of miscellaneous applications arithmetic algorithms and architectures DSP architectures systolic algorithms and architectures rapid prototyping design methodolgies and compilers **IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis** ,2005 *Proceedings, 4th IEEE International Symposium on High-Assurance Systems Engineering, November 17-19, 1999, Washington, D.C.* ,1999 Proceedings of the November 1999 symposium which focused on the development of embedded systems Examples of high assurance embedded applications are flight control systems medical surgery equipment military command systems vehicle braking components pacemakers traffic light control systems and satellites The major topics of the 24 papers are evaluation and testing fault analysis reliable communications frameworks systems and tools metrics and modeling and the use of UML in designing high assurance systems Case studies analyze the results of applying the latest research to real systems Three practical experience reports and 11 summaries from three panel discussions round out the volume No subject index Annotation copyrighted by Book News Inc Portland OR Proceedings of the 2000 Congress on Evolutionary Computation Institute of Electrical and Electronics Engineers,2000 These volumes contain the proceedings of the 2000 Congress on Evolutionary Computation The papers address genetic programming evolutionary optimization the evolution of neural networks evolutionary robotics data mining with evolutionary algorithms bio inspired hardware and more **ACM SIGPLAN Notices** ,2005-07 **Proceedings of the … International Symposium**

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