A Unified Approach for Timing Verification and Delay Fault Testing

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Unified Approach For Timing Verification And Delay Fault Testing:

A Unified Approach for Timing Verification and Delay Fault Testing Mukund Sivaraman,Andrzej J. Strojwas,2012-09-17 Large system complexities and operation under tight timing constraints in rapidly shrinking technologies have made it extremely important to ensure correct temporal behavior of modern day digital circuits both before and after fabrication Research in pre fabrication timing verification and post fabrication delay fault testing has evolved along largely disjoint lines in spite of the fact that they share many basic concepts A Unified Approach for Timing Verification and Delay Fault Testing applies concepts developed in the context of delay fault testing to path sensitization which allows an accurate timing analysis mechanism to be developed This path sensitization strategy is further applied for efficient delay fault diagnosis and delay fault coverage estimation A new path sensitization strategy called Signal Stabilization Time Analysis SSTA has been developed based on the fact that primitive PDFs determine the stabilization time of the circuit outputs This analysis has been used to develop a feasible method of identifying the primitive PDFs in a general multi level logic circuit An approach to determine the maximum circuit delay using this primitive PDF identification mechanism is also presented The Primitive PDF Identification based Timing Analysis PITA approach is proved to determine the maximum floating mode circuit delay exactly under any component delay model and provides several advantages over previously floating mode timing analyzers A framework for the diagnosis of circuit failures caused by distributed path delay faults is also presented A metric to quantify the diagnosability of a path delay fault for a test is also proposed Finally the book presents a very realistic metric for delay fault coverage which accounts for delay fault size distributions and is applicable to any delay fault model A Unified Approach for Timing Verification and Delay Fault Testing will be of interest to university and industry researchers in timing analysis and delay fault testing as well as EDA tool development engineers and design verification engineers dealing with timing issues in ULSI circuits The book should also be of interest to digital designers and others interested in knowing the state of the art in timing verification and delay fault testing **Delay Fault Testing for VLSI Circuits** Angela Krstic,Kwang-Ting (Tim) Cheng,2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader s understanding many key concepts are illustrated by simple examples

The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest

Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits M. Bushnell,Vishwani Agrawal,2006-04-11 The modern electronic testing has a forty year history Test professionals hold some fairly large conferences and numerous workshops have a journal and there are over one hundred books on testing Still a full course on testing is offered only at a few universities mostly by professors who have a research interest in this area Apparently most professors would not have taken a course on electronic testing when they were students Other than the computer engineering curriculum being too crowded the major reason cited for the absence of a course on electronic testing is the lack of a suitable textbook For VLSI the foundation was provided by semiconductor device techn ogy circuit design and electronic testing In a computer engineering curriculum therefore it is necessary that foundations should be taught before applications The field of VLSI has expanded to systems on a chip which include digital memory and mixed signalsubsystems To our knowledge this is the first textbook to cover all three types of electronic circuits We have written this textbook for an undergraduate foundations course on electronic testing Obviously it is too voluminous for a one semester course and a teacher will have to select from the topics We did not restrict such freedom because the selection may depend upon the individual expertise and interests Besides there is merit in having a larger book that will retain its usefulness for the owner even after the completion of the course With equal tenacity we address the needs of three other groups of readers **A Designer's Guide to Built-In Self-Test** Charles E. Stroud,2005-12-27 A recent technological advance is the art of designing circuits to test themselves referred to as a Built In Self Test This book is written from a designer s perspective and describes the major BIST approaches that have been proposed and implemented along with their advantages and limitations

Dependable Multicore Architectures at Nanoscale Marco Ottavi,Dimitris Gizopoulos,Salvatore Pontarelli,2017-08-28 This book provides comprehensive coverage of the dependability challenges in today s advanced computing systems It is an in depth discussion of all the technological and design level techniques that may be used to overcome these issues and analyzes various dependability assessment methods The impact of individual application scenarios on the definition of challenges and solutions is considered so that the designer can clearly assess the problems and adjust the solution based on the specifications in question The book is composed of three sections beginning with an introduction to current dependability challenges arising in complex computing systems implemented with nanoscale technologies and of the effect of the application scenario The second section details all the fault tolerance techniques that are applicable in the manufacture of reliable advanced computing devices Different levels from technology level fault avoidance to the use of error correcting codes and system level checkpointing are introduced and explained as applicable to the different application scenario

requirements Finally the third section proposes a roadmap of future trends in and perspectives on the dependability and manufacturability of advanced computing systems from the special point of view of industrial stakeholders Dependable Multicore Architectures at Nanoscale showcases the original ideas and concepts introduced into the field of nanoscale manufacturing and systems reliability over nearly four years of work within COST Action IC1103 MEDIAN a think tank with participants from 27 countries Academic researchers and graduate students working in multi core computer systems and their manufacture will find this book of interest as will industrial design and manufacturing engineers working in VLSI companies   **Principles of Testing Electronic Systems** Samiha Mourad,Yervant Zorian,2000-07-25 A pragmatic approach to testing electronic systems As we move ahead in the electronic age rapid changes in technology pose an ever increasing number of challenges in testing electronic products Many practicing engineers are involved in this arena but few have a chance to study the field in a systematic way learning takes place on the job By covering the fundamental disciplines in detail Principles of Testing Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today s very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references   Timing Verification of Application-specific Integrated Circuits (ASICs) Farzad Nekoogar,1999 PLEASE PROVIDE COURSE INFORMATION PLEASE PROVIDE   *Algebraic Methods for Timing Analysis and Testing in High Performance Designs* William Kwei-Cheung Lam,1993   **American Book Publishing Record** ,1998   **Dissertation Abstracts International** ,2004   *Proceedings* ,2001   **Fourth International Symposium on Quality Electronic Design** ,2003 ISQED looks into the research development and application of design techniques and methods design processes and EDA design methodologies and tools that address issues that impact the quality of the realization of designs into physical integrated circuits It emphasizes a holistic approach toward design quality and to highlight and accelerate cooperation among the IC Design EDA Semiconductor Process Technology and Manufacturing communities   **Science Abstracts** ,1995   *18th IEEE VLSI Test Symposium* ,2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test

compaction and design validation analog BIST and functional test and verification issues Also covered are STIL extension IDDQ test and on line testing and fault tolerance Lacks a subject index Annotation copyrighted by Book News Inc Portland OR *Proceedings of the ... American Control Conference* ,1995 **IEEE VLSI Test Symposium** ,2005 **13th Symposium on Integrated Circuits and Systems Design** Ricardo Augusto da Luz Reis,Jose Carlos Monteiro,Wilhelmus Van Noije,2000 These papers are taken from 13th Brazilian Symposium on Integrated Circuit Design SBCCI 2000 They address issues such as microarchitectures architecture logic design analogue design high level synthesis digital design physical modelling reconfigurable hardware and more *1987 IEEE Workshop on Languages for Automation* ,1987

Index to IEEE Publications Institute of Electrical and Electronics Engineers,1998 Issues for 1973 cover the entire IEEE technical literature **Twelfth International Conference on VLSI Design** VLSI Society of India,IEEE Circuits and Systems Society,1999 The proceedings of the January 1999 conference consist of 103 papers 11 talks and six tutorials The papers are grouped under the headings of TCAD to ECAD low power testing co design and synthesis analog design multi valued logic verification digital signal processor DSP logic synthesis

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