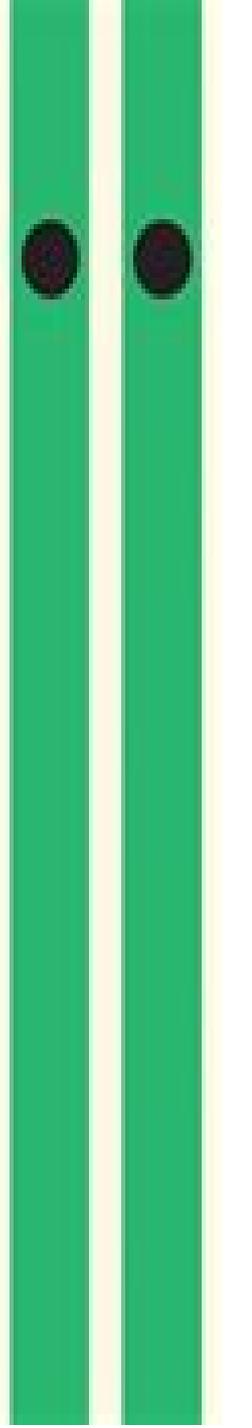
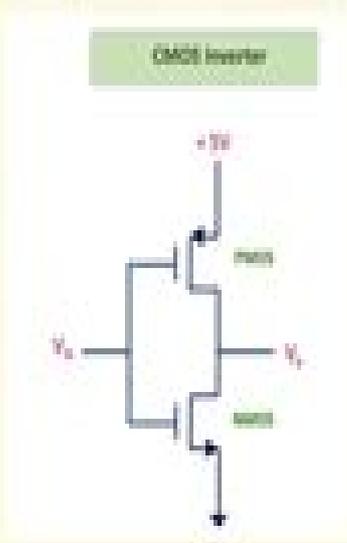


# CMOS - Overview

**CMOS stands for Complementary Metal-Oxide-Semiconductor. It's a technology used to make low-power, reliable electronic circuits for digital devices, including computers, microcontrollers, and memory chips.**

**CMOS is a type of metal-oxide-semiconductor field-effect transistor (MOSFET) fabrication process. It uses symmetrical pairs of p-type and n-type MOSFETs for logic functions.**



# Testing And Reliable Design Of Cmos Circuits

**Ubar, Raimund, Raik, Jaan, Vierhaus,  
Heinrich Theodor**

## **Testing And Reliable Design Of Cmos Circuits:**

Testing and Reliable Design of CMOS Circuits Niraj K. Jha, Sandip Kundu, 2012-12-06 In the last few years CMOS technology has become increasingly dominant for realizing Very Large Scale Integrated VLSI circuits. The popularity of this technology is due to its high density and low power requirement. The ability to realize very complex circuits on a single chip has brought about a revolution in the world of electronics and computers. However, the rapid advancements in this area pose many new problems in the area of testing. Testing has become a very time-consuming process. In order to ease the burden of testing, many schemes for designing the circuit for improved testability have been presented. These design for testability techniques have begun to catch the attention of chip manufacturers. The trend is towards placing increased emphasis on these techniques. Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults. In order to take care of this problem, we need to build fault-tolerant systems. The area of fault-tolerant computing has steadily gained in importance. Today many universities offer courses in the areas of digital system testing and fault-tolerant computing. Due to the importance of CMOS technology, a significant portion of these courses may be devoted to CMOS testing. This book has been written as a reference text for such courses offered at the senior or graduate level. Familiarity with logic design and switching theory is assumed. The book should also prove to be useful to professionals working in the semiconductor industry.

*Design and Test Technology for Dependable Systems-on-Chip* Ubar, Raimund, Raik, Jaan, Vierhaus, Heinrich Theodor, 2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC, Multi-Processor System on Chip MPSoC or Network on Chip NoC.

Introduction to Microelectronics to Nanoelectronics Manoj Kumar Majumder, Vijay Rao Kumbhare, Aditya Japa, Brajesh Kumar Kaushik, 2020-11-24 Focussing on micro and nanoelectronics design and technology, this book provides thorough analysis and demonstration starting from semiconductor devices to VLSI fabrication, designing analog and digital on-chip interconnect modeling culminating with emerging non-silicon nano-devices. It gives detailed description of both theoretical as well as industry standard HSPICE, Verilog, Cadence simulation-based real-time modeling approach with focus on fabrication of bulk and nano-devices. Each chapter of this proposed title starts with a brief introduction of the presented topic and ends with a summary indicating the futuristic aspect including practice questions. Aimed at researchers and senior undergraduate/graduate students in electrical and electronics engineering, microelectronics, nanoelectronics, and nanotechnology, this book provides broad and comprehensive coverage from Microelectronics to Nanoelectronics, including design in analog and digital electronics. Includes HDL and VLSI design going into the nanoelectronics arena. Discusses devices, circuit analysis, design methodology, and real-time simulation based on industry standard HSPICE tool. Explores emerging devices such as FinFETs, Tunnel FETs, TFETs, and CNTFETs, including their circuit co-designing. Covers real-time illustration using industry standard Verilog, Cadence, and Synopsys simulations.

Hierarchical Modeling for VLSI Circuit Testing Debashis Bhattacharya, John P. Hayes, 2012-12-06 Test generation is one of the most difficult tasks facing the designer of complex VLSI based digital systems Much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology It is long been recognized that the testing problem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation however the development of such methods has proceeded very slowly To be acceptable high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods The fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line SSL fault model which is tightly bound to the gate level of abstraction This monograph presents a novel approach to solving the foregoing problem It is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals A circuit is viewed as a collection of high level components such as adders multiplexers and registers interconnected by n bit buses To match this high level circuit model we introduce a high level bus fault that in effect replaces a large number of SSL faults and allows them to be tested in parallel However by reducing the bus size from n to one we can obtain the traditional gate level circuit and models

*Handbook of VLSI Chip Design and Expert Systems* A. F. Schwarz, 1993 Offers a conceptual and methodological understanding of chip design and of the fundamental principles in the computer aided design of VLSI circuits and systems CAD/CAS The text covers where why and how expert systems are used in subtasks of CAD/CAS and in the integrated chip design system

*On-Line Testing for VLSI* Michael Nicolaidis, Yervant Zorian, Dhiraj Pradhan, 2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers

International Test Conference, 1993, 1993    **VLSI design '91**, 1991    **Advanced Research in VLSI** Carlo H. Séquin, 1991 This conference is the thirteenth in a series that has been held at CalTech MIT University of North Carolina and Stanford Systems design and integration is the special focus of the 1991 conference

IEEE VLSI Test Symposium, 2001    **Proceedings of the ... European Test Conference**, 1993    *Encyclopedia of Computer Science and Technology* Allen Kent, James G.

Williams,1997-02-14 Artificial Intelligence in Economics and Managemetn to Requirements Engineering **19th IEEE VLSI Test Symposium** ,2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc *Proceedings* ,1994 **The Cumulative Book Index** ,1990 A world list of books in the English language A Probabilistic Analysis of Test Response Compaction Slawomir Pilarski,Tiko Kameda,1995 Synthesizes recent findings on the chance of missing a faulty circuit when the data from testing microelectronic systems is compacted to be more manageable a situation known as aliasing Considers single and multiple stuck at delay and stuck open faults Also reviews the testing of VLSI introduc *Neural Networks and Speech Processing* David P. Morgan,Christopher L. Scofield,1991-02-28 We would like to take this opportunity to thank all of those individ uals who helped us assemble this text including the people of Lockheed Sanders and Nestor Inc whose encouragement and support were greatly appreciated In addition we would like to thank the members of the Lab oratory for Engineering Man Machine Systems LEMS and the Center for Neural Science at Brown University for their frequent and helpful discussions on a number of topics discussed in this text Although we both attended Brown from 1983 to 1985 and had offices in the same building it is surprising that we did not meet until 1988 We also wish to thank Kluwer Academic Publishers for their profes sionalism and patience and the reviewers for their constructive criticism Thanks to John McCarthy for performing the final proof and to John Adcock Chip Bachmann Deborah Farrow Nathan Intrator Michael Perrone Ed Real Lance Riek and Paul Zemaný for their comments and assistance We would also like to thank Khrisna Nathan our most unbi ased and critical reviewer for his suggestions for improving the content and accuracy of this text A special thanks goes to Steve Hoffman who was instrumental in helping us perform the experiments described in Chapter 9 **Hardware Annealing in Analog VLSI Neurocomputing** Bank W. Lee,Bing J. Sheu,1990-12-31 Rapid advances in neural sciences and VLSI design technologies have provided an excellent means to boost the computational capability and efficiency of data and signal processing tasks by several orders of magnitude With massively parallel processing capabilities artificial neural networks can be used to solve many engineering and scientific problems Due to the optimized data communication structure for artificial intelligence applications a neurocomputer is considered as the most promising sixth generation computing machine Typical applica tions of artificial neural networks include associative

memory pattern classification early vision processing speech recognition image data compression and intelligent robot control VLSI neural circuits play an important role in exploring and exploiting the rich properties of artificial neural networks by using programmable synapses and gain adjustable neurons Basic building blocks of the analog VLSI neural networks consist of operational amplifiers as electronic neurons and synthesized resistors as electronic synapses The synapse weight information can be stored in the dynamically refreshed capacitors for medium term storage or in the floating gate of an EEPROM cell for long term storage The feedback path in the amplifier can continuously change the output neuron operation from the unity gain configuration to a high gain configuration The adjustability of the voltage gain in the output neurons allows the implementation of hardware annealing in analog VLSI neural chips to find optimal solutions very efficiently Both supervised learning and unsupervised learning can be implemented by using the programmable neural chips Integrated Circuit Design, Fabrication, and Test Peter Shepherd, 1996 All aspects of chip realization for both digital and analog circuits are covered Electronics engineers are shown how to choose appropriate technology and circuit architecture and plan the IC design They will gain expert information on power considerations the advantages and disadvantages of each IC architecture and aspects of design for testability **Seventh Annual IEEE International Conference on Wafer Scale Integration, San Francisco, California, USA** Glenn Chapman, Stuart Tewksbury, 1995

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