# Systolic Array Parallelizing Compiler

**Ping-Sheng Tseng**

**Systolic Array Parallelizing Compiler:**

**A Systolic Array Parallelizing Compiler** ,1990-08-31      A Systolic Array Parallelizing Compiler Ping-Sheng Tseng,2012-12-06 Widespread use of parallel processing will become a reality only if the process of porting applications to parallel computers can be largely automated Usually it is straightforward for a user to determine how an application can be mapped onto a parallel machine however the actual development of parallel code if done by hand is typically difficult and time consuming Parallelizing compilers which can gen erate parallel code automatically are therefore a key technology for parallel processing In this book Ping Sheng Tseng describes a parallelizing compiler for systolic arrays called AL Although parallelizing compilers are quite common for shared memory parallel machines the AL compiler is one of the first working parallelizing compilers for distributed memory machines of which systolic arrays are a special case The AL compiler takes advantage of the fine grain and high bandwidth interprocessor communication capabilities in a systolic architecture to generate efficient parallel code xii Foreword While capable of handling an important class of applications AL is not intended to be a general purpose parallelizing compiler      *A Systolic Array Optimizing Compiler* Monica S. Lam,2011-10-17 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high peiformance programmable systolic arrays represents a practical cost effective solu tion to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors      Parallel Computing and Transputers D. Arnold,1994 The broadening of interest in parellel computing and transputers is reflected in this text Topics covered include concurrent programming graphics and image processing and robotics and control It is based on the proceedings of the 6th Australian Transputer and Occam User Group      Opportunities and Constraints of Parallel Computing Jorge L.C. Sanz,2012-12-06 At the initiative of the IBM Almaden Research Center and the National Science Foundation a workshop on Opportunities and Constraints of Parallel Computing

was held in San Jose California on December 5 6 1988 The Steering Committee of the workshop consisted of Prof R Karp University of California at Berkeley Prof L Snyder University of Washington at Seattle and Dr J L C Sanz IBM Almaden Research Center This workshop was intended to provide a vehicle for interaction for people in the technical community actively engaged in research on parallel computing One major focus of the workshop was massive parallelism covering theory and models of computing algorithm design and analysis routing architectures and interconnection networks languages and application requirements More conventional issues involving the design and use of parallel computers with a few dozen processors were not addressed at the meeting A driving force behind the realization of this workshop was the need for interaction between theoreticians and practitioners of parallel computation Therefore a group of selected participants from the theory community was invited to attend together with well known colleagues actively involved in parallelism from national laboratories government agencies and industry *Programming Models for Massively Parallel Computers, 1993* Wolfgang Giloi,Stefan Jähnichen,Bruce D. Shriver,1993 Proceedings Parallel Computing **High-Performance VLSI Signal Processing Innovative Architectures and Algorithms, Algorithms and Architectures** K. J. Ray Liu,Kung Yao,1998 Electrical Engineering Signal Processing High Performance VLSI Signal Processing Innovative Architectures and Algorithms Volume 1 Algorithms and Architectures The first volume in a two volume set High Performance VLSI Signal Processing Innovative Architectures and Algorithms brings together the most innovative papers in the field focused introductory material and extensive references The editors present timely coverage of algorithm and design methodologies with an emphasis on today s rapidly evolving high speed architectures for VLSI implementations These volumes will serve as vital resources for engineers who want a comprehensive knowledge of the extremely interdisciplinary field of high performance VLSI processing The editors provide a practical understanding of the merits of total system design through an insightful synergistic presentation of methodology architecture and infrastructure Each volume features Major papers that span the wide range of research areas in the field Chapter introductions including historical perspectives Numerous applications oriented design examples Coverage of current and future technological trends Thorough treatment of high speed architectures *Research Projects in the Parallel Processing Laboratory* Scott B. Baden,1991 <u>Languages and Compilers for Parallel Computing</u> ,2003 **Languages and Compilers for Parallel Computing** Utpal Banerjee,1994 This book contains papers selected for presentation at the Sixth Annual Workshop on Languages and Compilers for Parallel Computing The workshop washosted by the Oregon Graduate Institute of Science and Technology All the major research efforts in parallel languages and compilersare represented in this workshop series The 36 papers in the volume aregrouped under nine headings dynamic data structures parallel languages High Performance Fortran loop transformation logic and dataflow language implementations fine grain parallelism scalar analysis parallelizing compilers and analysis of parallel programs The book represents a valuable snapshot of the state of research in the field in 1993 **High-performance Computing in**

**Engineering** H. Power,C. A. Brebbia,1995 A consideration of the use and the applications of supercomputers and parallel architectures for engineering purposes Topics covered include visco elastic finite element analysis performance convective heat transfer and integrated grid generation and viscous flow simulation    **Languages and Compilers for Parallel Computing** David Hillel Gelernter,Alexandru Nicolau,David A. Padua,1990 A collection of papers examining the languages and compilers for parallel computing It covers a wide variety of topics ranging from improving parallel program performance using critical path analysis to software engineering of parallel programs in the computation orientated display environment

   Languages and Compilers for Parallel Computing Zhiyuan Li,1998-04-29 This book constitutes the refereed proceedings of the 12th Biennial Conference of the Canadian Society for Computational Studies of Intelligence AI 98 held in Vancouver BC Canada in June 1998 The 28 revised full papers presented together with 10 extended abstracts were carefully reviewed and selected from a total of more than twice as many submissions The book is divided in topical sections on planning constraints search and databases applications genetic algorithms learning and natural language reasoning uncertainty and learning    *High Performance Compilers for Parallel Computing* Michael Joseph Wolfe,1996 Software Operating Systems

   **Parallel Functional Languages and Compilers** Bolesław Szymański,1991    **Compiler Transformations for Automatic Generation of VHDL from C for Code Acceleration on Reconfigurable Devices** Ayse Betul Buyukkurt,2008

   International aerospace abstracts ,1993    *Automatic Mapping of Multi-stage Algorithms Onto Distributed Memory Systems* Yin-Tsung Hwang,1993    **Computer, Communication and Networking Systems** K. R. Subramanian,E. S. Seumahu,1992 Network technology encompasses research addressing three major technological areas Basic Technology Applications and Management Integrated research into these three major fields viz computer systems communication systems and networking systems is the focus of this ICIE proceedings The papers presented are grouped into two volumes both of which will provide an often used technical reference to this key technology of the 1990s    **FPGA ...** ,2001

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