A Systolic Array Optimizing Compiler

Monica S. Lam

foreword by H.T. Kung

Systolic Array Optimizing Compiler

Karen A. Lemone

Systolic Array Optimizing Compiler:

   A Systolic Array Optimizing Compiler Monica S. Lam,2012-12-06 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high peiformance programmable systolic arrays represents a practical cost effective solu tion to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors   *A Systolic Array Optimizing Compiler* Monica S. Lam,2011-10-17 This book is a revision of my Ph D thesis dissertation submitted to Carnegie Mellon University in 1987 It documents the research and results of the compiler technology developed for the Warp machine Warp is a systolic array built out of custom high performance processors each of which can execute up to 10 million floating point operations per second 10 MFLOPS Under the direction of H T Kung the Warp machine matured from an academic experimental prototype to a commercial product of General Electric The Warp machine demonstrated that the scalable architecture of high peiformance programmable systolic arrays represents a practical cost effective solu tion to the present and future computation intensive applications The success of Warp led to the follow on iWarp project a joint project with Intel to develop a single chip 20 MFLOPS processor The availability of the highly integrated iWarp processor will have a significant impact on parallel computing One of the major challenges in the development of Warp was to build an optimizing compiler for the machine First the processors in the xx A Systolic Array Optimizing Compiler array cooperate at a fine granularity of parallelism interaction between processors must be considered in the generation of code for individual processors Second the individual processors themselves derive their performance from a VLIW Very Long Instruction Word instruction set and a high degree of internal pipelining and parallelism The compiler contains optimizations pertaining to the array level of parallelism as well as optimizations for the individual VLIW processors   A Systolic Array Optimizing Compiler M. S.-L. Lam,1987   A Systolic Array Parallelizing Compiler Ping-Sheng Tseng,1990-08-31 Widespread use of

parallel processing will become a reality only if the process of porting applications to parallel computers can be largely automated Usually it is straightforward for a user to determine how an application can be mapped onto a parallel machine however the actual development of parallel code if done by hand is typically difficult and time consuming Parallelizing compilers which can gen erate parallel code automatically are therefore a key technology for parallel processing In this book Ping Sheng Tseng describes a parallelizing compiler for systolic arrays called AL Although parallelizing compilers are quite common for shared memory parallel machines the AL compiler is one of the first working parallelizing compilers for distributed memory machines of which systolic arrays are a special case The AL compiler takes advantage of the fine grain and high bandwidth interprocessor communication capabilities in a systolic architecture to generate efficient parallel code xii Foreword While capable of handling an important class of applications AL is not intended to be a general purpose parallelizing compiler   *Parallel Supercomputing in MIMD Architectures* R.Michael Hord,2018-02-01 Parallel Supercomputing in MIMD Architectures is devoted to supercomputing on a wide variety of Multiple Instruction Multiple Data MIMD class parallel machines This book describes architectural concepts commercial and research hardware implementations major programming concepts algorithmic methods representative applications and benefits and drawbacks Commercial machines described include Connection Machine 5 NCUBE Butterfly Meiko Intel iPSC iPSC 2 and iWarp DSP3 Multimax Sequent and Teradata Research machines covered include the J Machine PAX Concert and ASP Operating systems languages translating sequential programs to parallel and semiautomatic parallelizing are aspects of MIMD software addressed in Parallel Supercomputing in MIMD Architectures MIMD issues such as scalability partitioning processor utilization and heterogenous networks are discussed as well This book is packed with important information and richly illustrated with diagrams and tables Parallel Supercomputing in MIMD Architectures is an essential reference for computer professionals program managers applications system designers scientists engineers and students in the computer sciences   *Parallel Computing and Transputers* D. Arnold,1994 The broadening of interest in parellel computing and transputers is reflected in this text Topics covered include concurrent programming graphics and image processing and robotics and control It is based on the proceedings of the 6th Australian Transputer and Occam User Group   **Conference Record of the Fifteenth Annual ACM Symposium on Principles of Programming Languages** ,1988   Encyclopedia of Parallel Computing David Padua,2014-07-08 Containing over 300 entries in an A Z format the Encyclopedia of Parallel Computing provides easy intuitive access to relevant information for professionals and researchers seeking access to any aspect within the broad field of parallel computing Topics for this comprehensive reference were selected written and peer reviewed by an international pool of distinguished researchers in the field The Encyclopedia is broad in scope covering machine organization programming languages algorithms and applications Within each area concepts designs and specific implementations are presented The highly structured essays in this work comprise synonyms a definition and discussion of the topic

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performance from a slowing technology curve Comprising 28 full length papers and a number of short poster papers this publication offers a high quality exploration of the current state of the art in the field It will be of particular interest to those involved in control structures and microprogramming processor architectures computer system implementation programming techniques and software engineering **Supercomputing 88: Technology assessment, industrial supercomputer outlooks, European supercomputing accomplishments, and performance & computations** ,1988

Parallel Functional Languages and Compilers Bolesław Szymański,1991

The Enigmatic Realm of **Systolic Array Optimizing Compiler**: Unleashing the Language is Inner Magic

In a fast-paced digital era where connections and knowledge intertwine, the enigmatic realm of language reveals its inherent magic. Its capacity to stir emotions, ignite contemplation, and catalyze profound transformations is nothing short of extraordinary. Within the captivating pages of **Systolic Array Optimizing Compiler** a literary masterpiece penned by way of a renowned author, readers embark on a transformative journey, unlocking the secrets and untapped potential embedded within each word. In this evaluation, we shall explore the book is core themes, assess its distinct writing style, and delve into its lasting effect on the hearts and minds of people who partake in its reading experience.

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