Matrix Computations on Systolic-Type Arrays

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   Systolic Computations M.A. Frumkin,2012-12-06 This monograph is devoted to a new method of parallel computing which uses VLSI technology in an effcient manner By this method data are fed to the cells of a systolic processor and results are obtained instantly Some theoretical and algorithmic questions which arise in the design of hardware and software for systolic processing are considered Special attention is devoted to the complexity of VLSI complexity of algorithms parallel algorithms relations between graphs of algorithms and graphs of processors parallel programming languages and the use of systolic algorithms for vector programming The book is unique for its inclusion of a library of systolic algorithms for solving problems from twelve branches of computer science and will be useful for designers of hardware and software for parallel processing   Concurrent Computations Stuart K. Tewksbury,Bradley Dickinson,Stuart C. Schwartz,2012-12-06 The 1987 Princeton Workshop on Algorithm Architecture and Technology Issues for Models of Concurrent Computation was organized as an interdisciplinary work shop emphasizing current research directions toward concurrent computing systems With participants from several different fields of specialization the workshop cov ered a wide variety of topics though by no means a complete cross section of issues in this rapidly moving field The papers included in this book were prepared for the workshop and taken together provide a view of the broad range of issues and alternative directions being explored To organize the various papers the book has been divided into five parts Part I considers new technology directions Part II emphasizes underlying theoretical issues Communication issues which are ad dressed in the majority of papers are specifically highlighted in Part III Part IV includes papers stressing the fault tolerance and reliability of systems Finally Part V includes systems oriented papers where the system ranges from VLSI circuits through powerful parallel computers Much of the initial planning of the workshop was completed through an informal AT T Bell Laboratories group consisting of Mehdi Hatamian Vijay Kumar Adri aan Ligtenberg Sailesh Rao P Subrahmanyam and myself We are grateful to Stuart Schwartz both for the support of Princeton University and for his orga nizing local arrangements for the workshop and to the members of the organizing committee whose recommendations for participants and discussion topics were par ticularly helpful A Rosenberg and A T   Transputing '91 Peter Welch,Toshiyasu L. Kunii,A. Bakkers,1991 Transputers constitute a revolutionary category of microprocessors for parallel processing which have become market leaders in 32 bit RISC architectures The wide range of applications has caused a multitude of activities of user groups in all major countries as well as regional activities on four continents For the first time the collaboration of all these user groups has let to the organization of a world conference Transputing 91   **Trace Theory and Systolic Computations** Martin Rem,1987   **Bit-level Systolic Arrays** Anthony John De Groot,1989   *The Application of a Sequence Notation to the Design of Systolic Computations* Rami Melhem,PITTSBURGH UNIV PA INST FOR COMPUTATIONAL MATHEMATICS AND APPLICATIONS.,1985 The sequence notation suggested in an earlier work provides a tool for the clear and precise

specification of systolic computations Namely it separates the static and dynamic levels of the specification At the static level the topology of the network and the function of each cell are described by a system of causal equations on sequences and at the dynamic level the data flow is described by the elements of the individual sequences This paper describes a method for the transformation of a given algorithm into a system of causal sequence equations input output description which specifies a systolic computation The basic idea of the method is to pack arrays of variables along one or more dimensions into sequences Doing this however may result in a system of equations that is not causal and hence a transformation of indices in the original algorithm may be essential in order to guarantee causality the positive increment of time **1985 International Symposium on VLSI Technology, Systems, and Applications** ,1985 *Mathematical Foundations of Computer Science* ,1984 **Supercomputers and Parallel Computation** D. J. Paddon,1984 Mathematical Foundations of Computer Science 1984 Michal Chytil,M.P. Chytil,V. Koubek,1984-08 **TENCON '93** ,1993 **Area-efficient VLSI Computation** Charles Eric Leiserson,1983 **Proceedings of the Seventeenth Hawaii International Conference on System Sciences 1984** James P. Fry,Bruce D. Shriver,1984 IEEE Proceedings of the Southeastcon ,1985 **Performance Prediction for Mapped Parallel Programs** Bernd Heinrich Stramm,1993 Proceedings of the ISMM International Conference: Parallel and Distributed Computing, and Systems R. Melhem,1992 *Parallel Processing Architectures and VLSI Hardware* Angel L. DeCegama,1989 High Speed Computing David Paul Casasent,1988 *Advanced Computer Architecture* D. P. Agrawal,1986 Computer architecture is expected to cover the gap between digital hardware and computer software This tutorial will emphasize the importance of such a close interaction and the impact of parallel distributed processing and VLSI technology will be clearly shown Other important issues include examination of tradeoffs in the design of supercomputers and potential advantages of unique architectural concepts Strategies for evaluating system performance will also be covered This tutorial is meant for system designers application engineers scientists researchers and students Some background in computer organization architecture will be assumed *Energy and Technology Review* ,1989

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