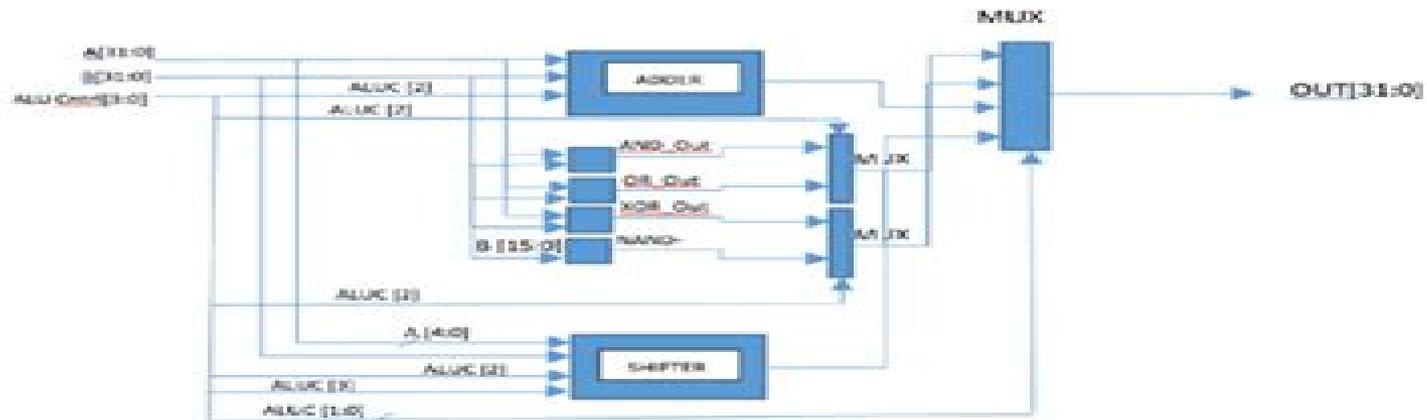


VLSI Architectures

Assignment 1 - Design of ALU

Yeshvanth M, 2023HT01517

High-level design in question



Solution

AND Gate

```

////////////////////////////////////
/* 32-bit AND Gate used in ALU */
: module AND
(
    input[31:0]  A_i,    // Input 1
    input[31:0]  B_i,    // Input 2
    output[31:0] AND_o  // AND result
);

    assign AND_o = A_i & B_i; // Behavioral modelling of AND gate
: endmodule

```

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N. Ranganathan



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