

# Cache memory



# The Cache Memory

**L Cohen**



## **The Cache Memory:**

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**Cache and Memory Hierarchy Design** Steven A. Przybylski, 1990 A widely read and authoritative book for hardware and software designers This innovative book exposes the characteristics of performance optimal single and multi level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time

**Official Gazette of the United States Patent and Trademark Office**, 2002

[The Cache-coherence Problem in Shared-memory Multiprocessors](#) Milo Tomašević, Veljko Milutinović, 1993 A tutorial on the nature of the cache coherence problem and the wide variety of proposed hardware solutions currently available A number of the most important papers in this field are included within seven sections introductory issues memory reference characteristics of parallel programs directo

*Cache-memory Interfaces in Compressed Memory Systems* International Business Machines Corporation. Research Division. (IBMRD), Caroline D.

Benveniste, Peter A. Franaszek, John T. Robinson, 2000 Abstract We consider a number of cache memory hierarchy design issues in systems with compressed random access memories C RAMs in which compression and decompression occur automatically to and from main memory Using a C RAM as main memory segments of main memory are stored in a compressed format and dynamically decompressed to handle cache misses at the next higher level of memory Design of main memory directory structures and storage allocation methods in such systems are described elsewhere here we focus on issues related to cache memory interfaces In particular if the cache line size of the cache or caches to which main memory data is transferred is different than the size of the unit of compression in main memory bandwidth and latency problems can occur Another issue is that of guaranteed forward progress that is ensuring that modified lines can be written to the compressed main memory so that the system can continue operation even if overall compression deteriorates We study several approaches for solving these problems using trace driven analysis to evaluate alternatives **Parallel and**

**Distributed Simulation Systems** Richard M. Fujimoto, 2000-01-03 From the preface page xv My goal in writing **Parallel and Distributed Simulation Systems** is to give an in depth treatment of technical issues concerning the execution of discrete event simulation programs on computing platforms composed of many processors interconnected through a network **SPARC**

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Proceedings Tencon, 1987 **Proceedings of the Trends in Electronics Conference**, 1987

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