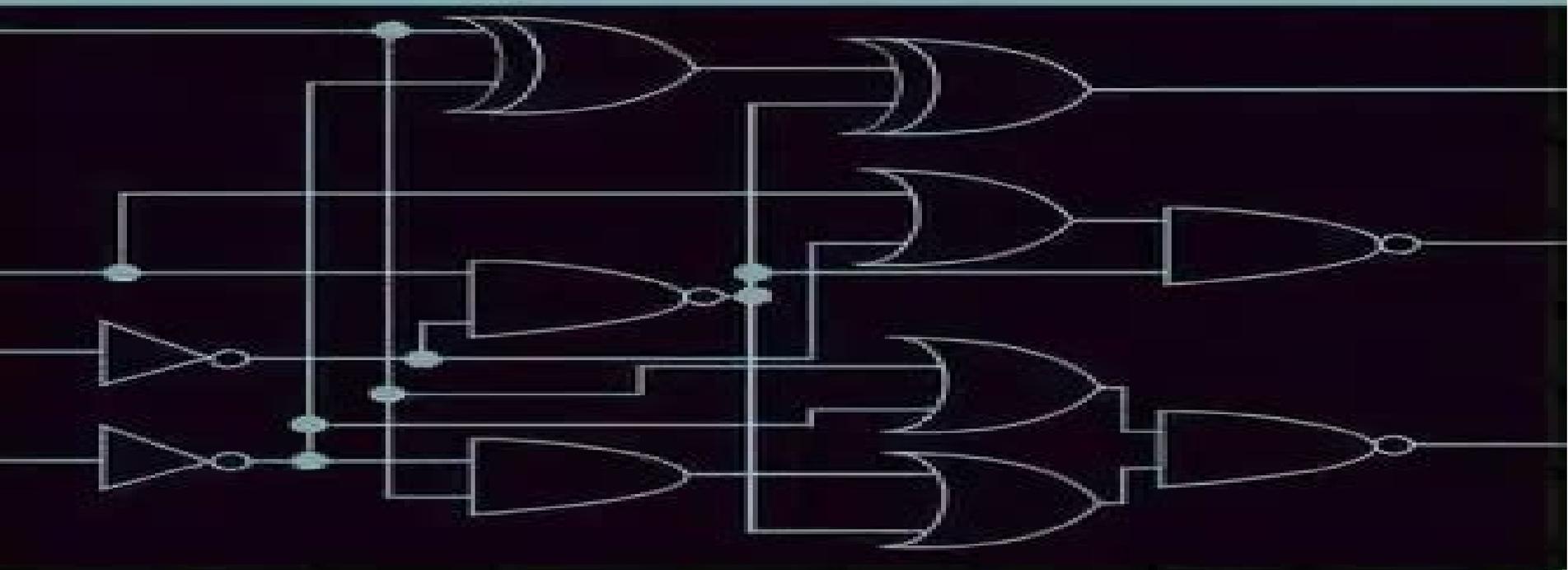


# Verilog Coding for Logic Synthesis

*Weng Fook Lee*



# Verilog Coding For Logic Synthesis

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